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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,919	04/16/2001	Hajime Akimoto	503.40029X00	5427

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EXAMINER	
KUMAR, SRILAKSHMI K	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/834,919	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the amendment filed on December 20, 2006.

Claims 1-39 are pending. Claims 28 and 29 have been amended.

Drawings

1. The drawings were received on 12/20/06. These drawings are approved by the examiner.

Specification

2. The substitute specification was received on 12/20/06. The changes made in the specification are approved by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. ***Claims 1, 9,* 11, 14-17, 21-23, 25, and 29-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,627,557) in view of Booth, Jr. et al., hereinafter Booth (U.S. Patent No. 6,642,915).

With reference to the **claim 1,** Yamaguchi et al. teaches a matrix of pixels (11 a) is disposed in the liquid crystal panel (11), wherein each pixel (11 a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 6719). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 46-55), wherein there is applied a refresh signal (see Fig. 16). Booth teaches a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element 9120), a circuit that stores a charge that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123) includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells

(125) automatically without receiving new image data, wherein each storage unit (124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125) (see column 5, lines 6-42). While also failing to teach the usage of a digital storage device, Booth does teach the usage of an optional D/A converter (103) (see column 4, lines 19-31), wherein it would be obvious to one having ordinary skill in the art to allow for the usage of a digital memory device when a D/A converter device is not included, in order to improve display intensity.

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device similar to that which is taught by Yamaguchi et al. which suggest usage of a refreshing signal in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display device that which the responding property of the liquid crystal is prevented from degrading.

With reference to **claim 9,** Yamaguchi et al. teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

With reference to **claim 11,** Yamaguchi teaches that the other end of the memory capacitor is connected to a wire to which a preset voltage (5) is applied.

With reference to **claims 12-14,** Yamaguchi teaches that the other end of the memory capacitor is connected to a drain of the amplifier (see Figures 1-2).

With reference to **claim 15,** Yamaguchi teaches that the drain of the amplifier FET is connected to a voltage applying means (GND) (see Figures 1-2).

With reference to **claim 16,** Yamaguchi teaches that the source of the amplifier is connected to the voltage applying means (see Figure 1-2).

With reference to **claims 17 and 25,** Yamaguchi teaches that the plurality of basic units of the memory elements are connected to the data lines, and the amplifier FET is connected to the data line through a switch (1).

With reference to **claims 21-23,** Yamaguchi fails to specifically teach that the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, wherein the memory switch and the selection switch in the individual units are connected to the same data line or data lines different from each other. Yamaguchi does teach that the pixels are arranged in a matrix and wherein elements (14, 15) have a single connection line that passes through each of the pixel elements. Moreover it is taught that the circuit structure of each pixel is not limited to the disclosed structure but includes the circuit structures according to other examples (see Fig. 14, column 15, lines 10-19).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the data line to connect both the memory switch and selection switch as taught by in by Yamaguchi or allow the memory switch and the selection switch to be connected to data lines different from each other as suggested by the teachings of Yamaguchi in order to provide a connection to the elements which allows the overall device to operated more efficiently.

With reference to **claim 26,** Yamaguchi et al. and Booth fail to specifically teach that the image signal generating means comprises a D/A converter. However, the Examiner takes

Official Notice that the usage of D/A converter is well known in the art for the data driver to include a D/A converter.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a D/A converter for converting the digital data in to analog data for further image processing.

With reference to **claims 29-31 and 36-38,** Yamaguchi et al. teaches a matrix of pixels (11 a) is disposed in the liquid crystal panel (11), wherein each pixel (11 a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

With further reference to **claims 32-35,** Yamaguchi et al. teaches amplifying a voltage level of the display data written in the data line and then rewriting the amplified voltage of the display data from the data line (see column 7, lines 25-34).

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 4655), wherein there is applied a refresh signal (see Fig. 16). Yamaguchi et al. fails to specifically teach refreshing by sequentially scanning, however the Examiner takes Official Notice that refreshing by a sequential scanning is a well-

known technique in the art and would have been obvious to one having ordinary skill in the art at the time of the invention to thereby provide improved refreshing for driving the image data.

Booth teaches a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element 9120), a circuit that stores a charge that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123) includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data. Booth also teaches that each storage unit 9124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125) (see column 5, lines 6-42).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device similar to that which is taught by Yamaguchi et al. which suggest usage of a refreshing signal in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display device that which the responding property of the liquid crystal is prevented from degrading.

6. ***Claims 2-8, 10, 18-20, 24, and 27*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. and Booth as applied to **claims 1, 9, 11, 14-17, 21-23, 25, and 29-39** above, and further in view of Parks (U.S. Patent No. 5,471,225).

With reference to **claims 2,** Yamaguchi et al. teaches a driving circuit (20) which is disposed in the peripheral portion of the liquid crystal panel (11) (see column 16, line 2-5).

Yamaguchi et al. and Booth fail to specifically teach that the liquid crystal region is formed between the pixel electrodes and the counter electrode.

Parks teaches the general construction of the LCD consisting of a pair of glass plates (22, 24), wherein the inside surface of glass panel (22) is a common electrode (30) and the inside of glass panel (24) is a pixel electrode wherein the liquid crystal (40) is located there between.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 3,** Yamaguchi et al. and Booth also fail to teach that the plurality of display pixels have an optical reflecting plate.

Parks teaches that the usage of alignment coatings and/or passivity coatings, are generally placed between electrode (30) and liquid crystal medium (40) as well as between each display electrode and liquid crystal medium.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 4,** Yamaguchi et al. teaches that the LC panel (11) occupies a display portion including a scanning signal and data signal line driver can be included in the display portion as shift registers (14, 15) and timing generating circuit (17) (see column 16, lines 12-17) thereby reducing the area need for the components, and in turn allowing the display area to be made smaller.

With reference to **claims 5 and 18-20,** Yamaguchi et al. teaches with reference to conventional art that the switching elements are TFTs (see column 1, lines 8-17).

With reference to **claims 6-8 and 10**, Yamaguchi teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

While Booth does teaches that the storage unit (124) may include a transistor that is activated to couple the capacitor to the pixel cell to refresh the terminal voltage across the pixel cell (see column 5, lines 33-38), the combination of Yamaguchi and Booth fail to teach that the switch or amplifier is of Poly-Si TFT type.

Parks teaches that the gate of the TFT is deposited upon the substrate accordingly to the well-known methods (see column 6, lines 36-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 24,** Yamaguchi et al. and Booth fail to specifically teach a black matrix shielding means arranged between the transparent substrate corresponding to the back

portions of the memory element and a lighting means. However, the Examiner takes Official Notice that the usage of a black matrix is well known in the art.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a black matrix in a device similar to that which is taught by the combination of Yamaguchi et al., Booth, and Parks in order to block unwanted light and thereby improving the contrast ratio of the display.

With reference to **claim 27**, Yamaguchi et al. and Booth fail to specifically teach that the image signal generating means comprises a D/A converter. However, the Examiner takes Official Notice that the usage of D/A converter is well known in the art for the data driver to include a D/A converter.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of a D/A converter for converting the digital data in to analog data for further image processing.

7. ***Claim 28*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Zhang et al. (U.S. Patent No. 6,611,261).

With reference to **claim 28**, Yamaguchi et al. teaches a matrix of pixels (11a) is disposed in the liquid crystal panel (11), wherein each pixel (11a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor

(CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Yamaguchi et al. fails the specific usage of an image signal generating means, which has a reference voltage generating circuit using a poly-Si thin film resistor as a gray scale voltage generating resistor.

Zhang et al. teaches a LCD device wherein it is disclosed the conventionality of using poly-silicon thin film transistors in LCD units and the peripheral circuits as well (see column 1, lines 15-20). It is further taught the usage of a D/A converter (350), which is comprised in the poly-Si digital driver, for generating gray scale signals based on the gray-scale reference voltage (see column 15, lines 42-57).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the combination of the poly-Si type image signal generating means as taught by Zhang et al. to be used in a device similar to that which is taught by Yamaguchi et al. in order to provide an improved arrangement for peripheral circuits of the display unit thereby allowing them to be formed as an integrated device.

Response to Arguments

8. Applicant's arguments filed 12/20/2006 have been fully considered but they are not persuasive.

With respect to the drawing corrections, these are approved by the examiner, as stated above.

With respect to the substituted specification, this is approved by the examiner, as stated above.

With respect to the prior art rejection, applicant argues on page 22 of the remarks, where the prior art of Yamaguchi and Booth fails to teach the claimed limitations including a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor as well as the teaching of a multi-bit digital memory device. The applicant states Yamaguchi discloses a display apparatus wherein a refresh is used to clear previous data, which has been read out from the image element capacitor. The applicant also states that Booth teaches storage units to regularly refresh the pixel cells automatically without receiving new image data. However the applicant believes that this is different from a refreshing operation means for performing an operation to rewrite a signal charge stored in the memory capacitor as recited in the claims. The examiner fails to see the difference in the claimed subject matter and the teaching of the combined references. The data stored in the memory element is refreshed, meaning that the data is changed from that which was initially stored. Therefore if the stored data of Yamaguchi is cancelled, cleared, or deleted, the data is changed from that which is initially stored thereby refreshing the stored data. Further Booth teaches that the display panel may use the storage units to regularly refresh the pixel cells automatically without receiving new image data. The applicant also argues intended usage of the refreshing operation in Booth, however intended usage is not being examined only the claimed limitations.

With respect to the applicant's arguments where the prior art fails to teach a display apparatus in which the image signal generating means has a reference voltage generating circuit using a poly-Si thin film resistor to achieve a gray scale voltage generating resistor. This feature is taught in the prior art of Zhang et al teaches a LCD device wherein it is disclosed the conventionality of using poly-silicon thin film transistors in LCD units and the peripheral circuits

as well (see column 1, lines 15-20). It is further taught the usage of a D/A converter (350), which is comprised in the poly-Si digital driver, for generating gray scale signals based on the gray-scale reference voltage (see column 15, lines 42-57). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the combination of the poly-Si type image signal generating means as taught by Zhang et al. to be used in a device similar to that which is taught by Yamaguchi et al. in order to provide an improved arrangement for peripheral circuits of the display unit thereby allowing them to be formed as an integrated device.

Therefore, the combination of the prior art teaches the limitations set forth in the instant application. Thus, the rejection is made FINAL.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

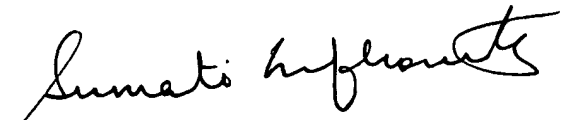
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K. Kumar
Examiner
Art Unit 2629

SKK
March 17, 2007



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